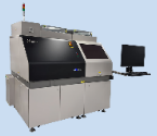
CMOS Sensor

Purpose	Inspection Solutions for CMOS Sensors to meet stringent assembly and final visual out going quality requirement.
Technology	1. **Sub Micron AOI** – Defect Size from 0.5um. Microscope objective, multiple direction illumination design combined field proven sub micron defect detection algorithm to detect sensor defects such as contamination, structure damage, fab defects. 2. **Macro AOI** – Defect Size from 5um. Packaged CMOS Sensors in JEDEC Tray. Inspection coverage includes all sides- Top, Bottom and Side walls defects. Offers capability to detect defects on glass defects, contamination, chipping and ceramic cracks 3. **Side Wall Inspection** – Inspect side wall defects include delamination, ceramic crack and void 4. **Void/Bubble Inspection** – Using Optical Interference technique to Detect surface topology variation caused by voids/bubbles between photodiode and top surface layers of CMOS image sensor 5. **Auto Defect Classification (ADC)** – Applying Rule and Region based automatic defect classification of defect signatures to identify, isolate and improve process issues.

STI Products	Sub Micron AOI	Macro AOI	Side Wall Inspection	Void/Bubble Inspection	ADC
 **iFocus – Wafer 2D & 3D Scan**	✓			✓	✓
 **Hexa – Tray 2D & 3D Scan**		✓	✓		
 **tScan – 2D & 3D High Speed Scan-Pack**		✓	✓		